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PATENT
Attorney Docket No.: BEA9-2000-0015-US1

BOARD OF PATENT APPEALS
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Davis et al.		
SERIAL NO.:	09/752,861	Group Art Unit:	2188
FILING DATE:	December 28, 2000		
FOR:	**NUMA System Resource Descriptors Including Performance Characteristics**	Examiner:	Portka, G.

TRANSMITTAL LETTER

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Rochelle Lieberman, Reg. No. 39,276

Enclosed is a corrected Brief in Support of Appeal pursuant to the communication of December 23, 2005. Copies of all references which were relied upon by Appellant and a payment pursuant to 37 C.F.R. §1.17(c) were submitted with the original Brief in Support of Appeal on March 25, 2005.

Respectfully submitted,

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BRIEF OF PATENT OWNER ON APPEAL

1. *Real Party in Interest*

International Business Machines Corporation, a New York corporation, is the real party in interest.

2. *Related Appeals and Interferences*

There are no related appeals or interferences.

3. *Status of Claims*

Claims 1-28 remain pending in the application. Claims 1, 3, 10, 13, and 22 were

amended in response to the First Office Action dated August 23, 2004. The claims on Appeal are included in the Appendix.

4. *Status of Amendments*

Amendments to claims 9, 12, 18, 21, 25, and 26 were submitted after final rejection.

5. *Summary of Claimed Subject Matter*

Applicant's invention is a computer system that utilizes a set of data structures to model data paths. Firmware is used to create the data structures which in turn identify where each resource is located within the system topology. The firmware is used to store topology information in a data structure. Pointers are added to the data structure for addressing additional functions, which are maintained in the form of secondary data structures. An extended system descriptor is produced by the firmware to maintain information pertaining to the nodes in the system, a pointer to a node descriptor, information pertaining to the quantity of system interconnect levels, and an average system interconnect latency table. The extended system descriptor is also in the form of a data structure which stores a primary level of the system or partition layout, and includes pointers to another level of data structures for each node within the system. The extended system descriptor references a node descriptor data structure, which includes pointers to an array of secondary data structures. The extended system descriptor is the primary data structure over the physical layout of the node in the system, and includes a pointer to the node descriptor data structure, which in turn includes pointers to another level of data structures representing each of the resources in a node. In addition, a memory map is included to reference the memory blocks of each node. Accordingly, the firmware herein is a data structure containing information pertaining to the layout and topology of the computer system and the resources therein.

With respect to claim 1, support for the elements in line 2 of the body of the claim is found in the original specification on page 5, lines 5-6, support for the elements in line 3 of the

body of the claim is found in the original specification on page 5, lines 9-14, support for the elements in line 4 of the body of the claim is found in the original specification on page 6, lines 24-30 and page 7, lines 17-18, support for the elements in line 5 of the body of the claim is found in the original specification on page 7, lines 18-29, and support for the elements in line 6 of the body of the claim is found on page 4, lines 22-25.

With respect to claim 13, support for the elements in line 2 of the body of the claim is found on page 5, lines 9-14, support for the elements found on line 3 of the body of the claim is found on page 6, lines 25-30 and page 7, lines 25-29, support for the elements found in line 4 of the body of the claim is found on page 11, lines 22-29 and page 12, lines 13-23, and support for the elements found in line 5 of the body of the claim is found on page 15, lines 10-12.

With respect to claim 22, support for the elements in line 2 of the body of the claim is found on page 5, lines 11-14, and support for the elements in lines 3 and 4 of the body of the claims is found on page 4, lines 19-25 and page 6, lines 20-21.

6. *Grounds of Rejection To Be Reviewed On Appeal*

Whether claims 1, 4, 5, 13-17, 22-24, and 28 are unpatentable over *Elnozahy et al.*, U.S. Patent No. 6,701,421, in view of *Sayles*, U.S. Patent No. 6,549,963, under 35 U.S.C. §103(a).

Whether claims 2, 3, 9-12, 18-21, and 25-27 are unpatentable over *Elnozahy et al.*, U.S. Patent No. 6,701,421, in view of *Sayles*, U.S. Patent No. 6,549,963, under 35 U.S.C. §103(a).

Whether claims 6, 7, and 8 are unpatentable over *Elnozahy et al.*, U.S. Patent No. 6,701,421, in view of *Sayles*, U.S. Patent No. 6,549,963, under 35 U.S.C. §103(a).

7. *ARGUMENT*

I. Rejection of Claims 1, 4, 5, 13-17, 22-24, and 28 under 35 U.S.C. §103(a).

In the Official Action of October 26, 2004, the Examiner rejected claims 1, 4, 5, 13-17, 22-24, and 28 under 35 U.S.C. §103(a) as being unpatentable over *Elnozahy et al.*, U.S. Patent No. 6,701,421, in view of *Sayles*, U.S. Patent No. 6,549,963. The U.S. Supreme Court set forth the factual inquiries in determining obviousness under 35 U.S.C. §103(a) as follows:

1. Determining the scope and contents of the prior art;
2. Ascertaining the differences between the prior art and the claims at issue;
3. Resolving the level of ordinary skill in the pertinent art; and
4. Considering objective evidence present in the application indicating obviousness or non-obviousness in view of the first three factors.

Graham v. John Deere Co., 383 U.S. 1, 17-18 (1966).[1] In following this factual inquiry, the Examiner must first consider the scope and contents of the prior art.

A. Discussion of the Contents of the Prior Art Reference Cited by the Examiner.

In rejecting claims 1, 4, 5, 13-17, 22-24, and 28 under 35 U.S.C. §103(a) as being unpatentable over *Elnozahy et al.*, in view of *Sayles*, the Examiner is hypothetically applying a method for allocating data with a method for configuring devices through the use of Basic Input Output System (BIOS).

The *Elnozahy et al.* patent shows a NUMA computer system that includes a set of nodes, with each node having processors, system memory, and a standard set of peripheral devices. Fig. 3 illustrates selected components of software used in the NUMA system. As illustrated, the software components include Basic Input Output System (BIOS) which is responsible for creating configuration tables that identify hardware components of the system and the size of the system memory. See Col. 4, lines 6-9. Accordingly, the computer system of *Elnozahy et al.* supports a computer system with BIOS for generating a configuration table in response to a boot event, wherein the configuration table identifies the system's hardware resources.

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[1] Applicant wishes to note that the U.S. Supreme Court in *Graham v. John Deere Co.* set forth a three part factual inquiry under 35 U.S.C. §103. Examiner's noted fourth part is merely recognized as the analysis of the results of the first three parts of the inquiry noted here.

The *Sayles* patent shows a computer system having a bus coupled to multiple devices having different communications characteristics. At start up, a BIOS routine may be used to change settings in devices coupled to the bus to indicate which transfer modes are supported. See Col. 3, lines 15-16. Fig. 3 illustrates the BIOS routines initialization of tasks. The BIOS routine may be programmed to change communication settings in the bus, to determine if more than two devices are located on the bus, and/or to indicate supported transfer modes of the bus. Accordingly, the BIOS of *Sayles* is used to changes settings associated with a bus.

B. Differences between the prior art and the claims at issue

In reviewing and studying the prior art references of *Elnozahy et al.* and *Sayles* it is clear that the scope of the contents are divergent in nature. The *Elnozahy et al.* patent accounts for a configuration table to identify hardware components of a computer system. However, there is no consideration given to expand the configuration table beyond identification. In fact, the *Elnozahy et al.* patent does not teach or suggest expansion of the system by including an additional descriptor pertaining to respective performance of resources in the system. Accordingly, *Elnozahy et al.* fails to account for a second descriptor produced by firmware as claimed by Applicant, wherein the second descriptor pertains to performance of resources within the system.

The *Sayles* patent accounts for BIOS to change settings in a bus of a computer system. However, there is no consideration in the *Sayles* patent for another descriptor associated with topological levels of one or more resources in the system. In fact, the *Sayles* patent does not teach or suggest expansion of the system by including an additional descriptor pertaining to topological levels of resources in the system. Accordingly, *Sayles* fails to account for an additional descriptor produced by firmware as claimed by Applicant, wherein the additional descriptor pertains to topological levels of one or more of the resources within the system.

C. Discussion of Applicant's Invention in View of the Prior Art References and Prior

Art References Failure to Teach, Suggest, or Motivate the Claimed Combination

There is no teaching in *Elnozahy et al.* for firmware to produce first and second descriptors. At most, *Elnozahy et al.* teaches firmware to produce only one of the two descriptors. Similarly, there is no teaching in *Sayles* for firmware to produce first and second descriptors. At most *Sayles* teaches only one of the two descriptors. In order to apply *Elnozahy et al.* to Applicant's pending application, *Elnozahy et al.* must be modified and reconfigured to support the firmware producing the two descriptors of Applicants. However, having the firmware produce the two descriptors of Applicants goes against the teachings of *Elnozahy et al.* "Although a prior art device 'may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so.' " MPEP §2143.01 (citing *In re Mills*, 916 F.2d 680, 682, 16 USPQ2d 1430 (Fed. Cir. 1990). *Elnozahy et al.* does not teach or suggest firmware configured to produce the two descriptors as claimed by Applicant. To read *Elnozahy et al.* as providing or supporting both of these elements would require a modification to the invention of *Elnozahy et al.* not envisioned or required. Similarly, to read *Sayles* as providing firmware to produce the two descriptors claimed by Applicant would require a modification to the invention of *Sayles* not envisioned or required. The only suggestion for firmware that produces the two descriptors is derived from Applicant's invention. Absent Applicant's invention, there is no suggestion or motivation within *Elnozahy et al.* or *Sayles* for such modifications. "It is impermissible to use the claimed invention as an instructions manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780 (Fed. Cir. 1992) (citing *In re Gorman*, 933 F.2d 982, 987 (Fed. Cir. 1991)). Yet this is the very process that the Examiner has attempted to undertake. Although Applicant's invention may appear to combine elements found in *Elnozahy et al.* and *Sayles*, "the inquiry under [35 U.S.C.] §103 is whether prior use makes the picture of the jigsaw puzzle, rather than its piece obvious." *Kori Corp. v. Wilco Marsh Buggies & Draglines*, 708 F.2d 151, 155 (5th Cir. 1983). The entirety of Applicant's invention is greater than the sum of the parts that comprise the novelty of the invention. "[T]he linchpin is not whether the individual components of the patent were obvious at the time of the invention, but whether the aggregation produced a new or different result or

achieved a synergistic effect." *Id.* (Citing Continental Oil Co. v. Cole, 634 F.2d 188, 197 (5th Cir. 1981). Unlike *Elnozahy et al.* or *Sayles*, Applicant's firmware is configured to produce two descriptors, a first descriptor reflecting topology and a second descriptor reflecting performance of resources. It is the dynamic characteristic of the firmware together with the claimed descriptors that enhance system performance.

Even if for the purposes of argument it would be trivial to combine the teachings of *Elnozahy et al.* with the teachings of *Sayles*, it would not necessarily be obvious to combine them in view of one another. There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. See MPEP §2143. "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure." MPEP §2143, (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Here *Elnozahy et al.* teaches the use the first descriptor, but does not teach, suggest, or motivate to expand beyond the first descriptor. As noted by the Examiner, *Elnozahy et al.* fails to teach or suggest the second descriptor produced by firmware. While *Sayles* teaches the second descriptor, there is no suggestion of employing a first descriptor, or an equivalent thereof, by firmware. "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art suggests the desirability of the combination." MPEP §2143.01 (citing *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)). The only suggestion for the combination of elements that form Applicant's invention is found in Applicant's invention itself. Accordingly, the Applicant respectfully submits that claims 1, 4-5, 13-17, 22-24, and 28 would not have been obvious for the above outlined reasons and a ruling by the Board of Patent Appeals in Applicant's favor and allowance of claims 1, 4-5, 13-17, 22-24, and 28 is respectfully requested.

II. Rejection of Claims 2, 3, 9-12, 18-21, and 25-27 under 35 U.S.C. §103(a).

In the Official Action of October 26, 2004, the Examiner rejected claims 2, 3, 9-12, 18-21, and 25-27 under 35 U.S.C. §103(a) as being unpatentable over *Elnozahy et al.*, U.S. Patent No. 6,701,421, in view of *Sayles*, U.S. Patent No. 6,549,963.

The discussions and comments pertaining to *Elnozahy et al.* and *Sayles* above are hereby incorporated by reference.

A. Differences between the prior art and the claims at issue

In reviewing and studying the prior art references of *Elnozahy et al.* and *Sayles*, it is clear that although each of *Elnozahy et al.* and *Sayles* may contain some of the elements of Applicant's invention, individually or in combination they do not teach all of the claimed elements.

B. Discussion of Applicant's Invention in View of the Prior Art References and Prior Art References Failure to Teach All of the Claimed Limitations of Applicant's Invention

As the CAFC has made clear, the prior art must teach the desirability of the modification. "The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification." *In re Gordon et al.*, 733 F.2d 900, 221 USPQ 1125, 1127 (Fed. Cir. 1984). It is axiomatic that the subject matter of the claims may not be considered obvious as a result of a hypothetical combination of references unless something in the references suggests that an advantage may be derived from combining their teachings. In this respect, the CAFC appears to speak directly to the issue of the need to determine the scope and contents of the prior art. Accordingly, the determination as to what may be within the scope and contents of the prior art serves to establish the parameters of what art may even be considered in determining the obviousness of an invention.

As noted above, each of *Elnozahy et al.* and *Sayles* patents may individually contain some of the elements of Applicant's invention. However, neither *Elnozahy et al.* nor *Sayles* teach or suggest any of their supposed first and second descriptors in the form of a data structure. In order to apply *Elnozahy et al.* and/or *Sayles* to Applicant's pending application, *Elnozahy et al.* and/or *Sayles* must be modified and reconfigured in order to support a modification of firmware from the traditional computer system to a data structure format. "To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art."

MPEP §2143.03, citing *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Both *Elnozahy et al.* and *Sayles* clearly do not show a format of the first descriptor as a data structure or a format of the second descriptor as a data structure. In order to provide the data structure format of the descriptors produced by the firmware, the systems of both *Elnozahy et al.* and *Sayles* must be modified in such a way as to provide the data structure format. However, this goes against the teaching of both *Elnozahy et al.* and *Sayles*, individually and in combination, with respect to the prior art. "Although a prior art device 'may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so'." MPEP §2143.01 (citing *In re Mills*, 916 F.2d 680, 682, 16 USPQ 2d. 1430 (Fed. Cir. 1990)). Neither *Elnozahy et al.* nor *Sayles* suggest a data structure format for the associated descriptors. To read either *Elnozahy et al.* or *Sayles* as providing such would require a modification to each of the inventions of *Elnozahy et al.* and *Sayles* not envisioned or required. The only suggestion for utilizing firmware to produce first and second descriptors in the form of data structures is derived from Applicant's invention. Absent Applicant's invention, there is no teaching, suggestion, or motivation within *Elnozahy et al.* or *Sayles* for such a modification. Unlike *Elnozahy et al.* and *Sayles*, Applicant's invention modifies the firmware into a plurality of data structures to provide a novel system for enabling intelligent decisions regarding placement of workload with respect to resources. Accordingly, Applicant respectfully contends that the teachings of *Elnozahy et al.* and *Sayles* do not meet the standard set by the CAFC's interpretation of 35 U.S.C. §103(a), and respectfully requests the Board of Patent Appeals rule in Applicant's favor and direct allowance of claims 2, 3, 9-12, 18-21, and 25-27.

III. Rejection of Claims 6, 7, and 8 under 35 U.S.C. §103(a).

In the Official Action of October 26, 2004, the Examiner rejected claims 6, 7, and 8 under 35 U.S.C. §103(a) as being unpatentable over *Elnozahy et al.*, U.S. Patent No. 6,701,421, in view of *Sayles*, U.S. Patent No. 6,549,963.

The discussions and comments pertaining to *Elnozahy et al.* and *Sayles* above are hereby incorporated by reference.

A. Differences between the prior art and the claims at issue

In reviewing and studying the prior art references of *Elnozahy et al.* and *Sayles*, it is clear that although each of *Elnozahy et al.* and *Sayles* may contain some of the elements of Applicant's invention, individually or in combination they do not teach all of the claimed elements. More specifically, the elements of claims 6, 7, and 8 focus on a dynamic updator for both the first and second descriptors and the functionality associated therewith. Even if one were to equivocate the hardware abstraction layer of *Elnozahy et al.* with the first descriptor, there remains no support for a second descriptor nor a dynamic updator for the second descriptor.

B. Discussion of Applicant's Invention in View of the Prior Art References and Prior Art References Failure to Teach All of the Claimed Limitations of Applicant's Invention

As noted above, each of *Elnozahy et al.* and *Sayles* patent may individually contain some of the elements of Applicant's invention. However, neither *Elnozahy et al.* nor *Sayles* make reference or implication of a dynamic updator. Although the hardware abstraction layer of *Elnozahy et al.* may be used to update the BIOS, there is no support for the hardware abstraction layer to update a second descriptor in a dynamic manner. In order to apply *Elnozahy et al.* to the elements of claims 6-8, the system of *Elnozahy et al.* must be modified in such a way as to provide two descriptors and a dynamic updator for both of the descriptors. However, this goes against the teaching of both *Elnozahy et al.* and *Sayles*, individually and in combination, with respect to the prior art. "Although a prior art device 'may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so'." MPEP §2143.01 (citing *In re Mills*, 916 F.2d 680, 682, 16 USPQ 2d. 1430 (Fed. Cir. 1990)). Neither *Elnozahy et al.* and *Sayles* suggest a system with two descriptors produced by the firmware and a dynamic updator for both of the claimed descriptors. To read either or both *Elnozahy et al.* or *Sayles* as providing such would require a modification to each of the

inventions of *Elnozahy et al.* and *Sayles* not envisioned or required. The only suggestion for utilizing a dynamic updator to both the first and second descriptors is derived from Applicant's invention. Absent Applicant's invention, there is no suggestion or motivation within *Elnozahy et al.* or *Sayles* for such a modification. "It is impermissible to use the claimed invention as an instruction manual or 'template' to piece togther the teachings of the prior art so that the claimed invention is rendered obvious." *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ 2d 1780 (Fed. Cir. 1992) (citing *In re Gorman*, 933 F.2d 982, 987 (Fed. Cir. 1991)). Yet this is the very process that the Examiner has attempted to undertake. The entirety of Applicant's invention is greater than the sum of the parts that comprise the novelty of the invention. Unlike *Elnozahy et al.* and *Sayles*, Applicant's invention does include a dynamic updator to the first and second descriptors to support updating the descriptors during operation of the computer system. Accordingly, Applicant respectfully contends that the teachings of *Elnozahy et al.* and *Sayles* do not meet the standard set by the CAFC's interpretation of 35 U.S.C. §103(a), and respectfully requests the Board of Patent Appeals rule in Applicant's favor and direct allowance of claims 6-8.

C. Discussion of Applicant's Invention in View of the Prior Art References and Prior Art References Failure to Teach All of the Claimed Limitations of Applicant's Invention.

The discussion of *Elnozahy et al.* and *Sayles* above is hereby incorporated by reference. As noted above, Applicant respectfully submits that the limitations of Applicant's claimed invention would not have been obvious for the reasons discussed in Section I above. Accordingly, Applicant respectfully requests a ruling by the Board of Patent Appeals and Interferences in Applicant's favor and allowance of claim 6-8.

In reviewing and studying the prior art reference of *Elnozahy et al.* and *Sayles*, it is clear that these references do not touch on a dynamic updator for both the first and second descriptors as taught by Applicant. The *Elnozahy et al.* patent accounts for at most one of the descriptors

and potentially a dynamic updator associated therewith, and the *Sayles* patent accounts for at most the other descriptor. There is no suggestion within the prior art for a computer system that employs both descriptors and a dynamic updator for both of the descriptors. "To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." MPEP §2143.03 (citing *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)). Clearly, the *Elnozahy et al.* patent does not teach the limitation of expanding the alleged updator to a second descriptor since there is no teaching, suggestion, or motivation within *Elnozahy et al.* for a second descriptor. Similarly, there is no teaching, suggestion, or motivation with *Sayles* to provide a dynamic updator to the alleged descriptor. Accordingly, Applicant respectfully submits that claims 6-8 would not have been obvious for the above outlined reasons and a ruling by the Board of Patent Appeals and Interferences in Applicant's favor and allowance of claims 6-8 is respectfully requested.

D. Discussion of Applicant's Invention in View of the Prior Art References and Prior Art References Failure to Teach the Desirability of Applicant's Invention.

The discussion of *Elnozahy et al.* and *Sayles* above are hereby incorporated by reference. As noted above, Applicant respectfully submit that the limitations of Applicant's claimed invention would not have been obvious for the reasons discussed in Section I above regarding *Elnozahy et al.* and *Sayles* and this Section III. Applicant contends that the prior discussion clearly mitigates in favor of concluding that the prior art reference utilized by the Examiner fail to teach the desirability of Applicant's invention. Accordingly, Applicant respectfully requests a ruling by the Board of Patent Appeals and Interferences in Applicant's favor and allowance of claims 6-8.

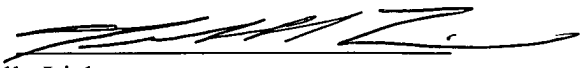
IV. Conclusion

In view of the rejections presented by the Examiner in the Office Action made final, it appears clear on the record that the *Elnozahy et al.* and *Sayles* references do not obviate

Applicant's invention based upon the legal definition of obviousness. Although the prior art reference cited by the Examiner relates to a computer system having alleged descriptor or equivalents thereof, the structure of the descriptors of *Elnozahy et al.* and *Sayles* are different than that claimed by Applicants. Neither *Elnozahy et al.* nor *Sayles* exhibits the motivation or suggest the desirability of modifications present such that one skilled in the art would find it obvious to incorporate modifications to enhance system performance as claimed by Applicant. In fact, neither *Elnozahy et al.* nor *Sayles* mentions or suggests expansion to an additional descriptor, nor do they teach or suggest a data structure format for each of the descriptors. Accordingly, as noted above, it is improper to use Applicant's claimed invention as a template for hindsight reconstruction or as the very means for drawing to the obviousness of the claimed invention even if that could construct the claimed invention where the prior art is otherwise not analogous or does not suggest the desirability for one skilled in the art to incorporate such modifications.

Applicant believes that those skilled in the art have failed to solve the problem as claimed by Applicant. Accordingly, for the reasons outlined above, Applicant respectfully requests the Board of Patent Appeals direct allowance of this application and all pending claims.

Respectfully submitted,

By: 
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Date: January 23, 2006

8. Claim Appendix:

1. A computer system, comprising:
multiple processors;
a plurality of resources assigned to node groups;
a first descriptor of respective topological levels of at least one of the resources; and
a second descriptor of respective performance of said resources,
wherein the first and second descriptors are produced by firmware.

2. The system of claim 1, wherein said descriptor is a first level data structure, and said second descriptor is a primary data structure.

3. The system of claim 2, wherein said primary data structure comprises a pointer to a secondary data structure.

4. The system of claim 1, further comprising a node identifier for each node for identifying positional placement of a resource.

5. The system of claim 4, wherein said node identifier represents multiple levels of interconnect.

6. The system of claim 1, further comprising a dynamic updator of at least the first and second descriptors.

7. The system of claim 6, wherein said dynamic updator reflects real-time system configuration into the first descriptor.

8. The system of claim 6, wherein said dynamic updator reflects real-time system performance into the second descriptor.

9. The system of claim 1, wherein said second descriptor includes a pointer to a secondary data structure having a descriptor selected from the group consisting of: processor descriptors, bus descriptors, memory descriptors, and share cache descriptors.

10. The system of claim 9, wherein said shared cache descriptor reflects interconnects of the system.

11. The system of claim 10, wherein said shared cache descriptor reflects latencies of the interconnects.

12. The system of claim 1, wherein said first descriptor reflects average latency between the node groups.

13. An article comprising:

a computer-readable signal bearing medium readable by a computer having multiple processors and a plurality of resources assigned to node groups;

means in the medium for determining topological levels of at least some of the resources; and

means in the medium for determining performance of said resources,

wherein said topological level determining means and said performance determining means are capable of being stored in firmware of the system.

14. The article of claim 13, wherein the medium is a recordable data storage medium.

15. The article of claim 13, wherein the medium is a modulated carrier signal.

16. The article of claim 13, wherein said topological level determining means is a first descriptor and said performance determining means is a second descriptor.

17. The article of claim 13, further comprising a node identifier for identifying positional

placement of a resource for each node.

18. The article of claim 16, wherein said second descriptor is selected from the group consisting of: processor descriptors, bus descriptors, memory descriptors, and share cache descriptors.

19. The article of claim 13, wherein said second descriptor comprises a shared cache descriptor which reflects interconnect of resources.

20. The article of claim 19, wherein said shared cache descriptor reflects latencies of the interconnects.

21. The article of claim 16, wherein said second descriptor reflects average latencies between node groups.

22. A method for enabling allocation of resources in a multiprocessor, comprising:

assigning multiple resources into node groups; and

maintaining system resource topology and performance descriptions as at least one data structure produce by firmware.

23. The method of claim 22, further comprising traversing the data structure to enable allocation of at least some of the resources.

24. The method of claim 22, wherein said traversal step includes accessing a second data structure.

25. The method of claim 24, wherein said second data structure is selected from the group consisting of: processor descriptors, bus descriptors, memory descriptors and shared cache descriptors.

26. The method of claim 24, wherein said second data structure includes a shared cache descriptor for describing at least part of a system interconnect including latency between sibling nodes.

27. The method of claim 22, further comprising maintaining at least average latency between at least two of the nodes.

28. The method of claim 22, wherein said traversal step includes recursively accessing additional data structure levels.

9. *Evidence Appendix*

Graham V. John Deere Co., 383 U.S. 1 (1966)

MPEP §2143.01

In re Gordon et al., 733 F.2d 900, 221 USPQ 1125, 1127 (Fed. Cir. 1984)

In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780 (Fed. Cir. 1992) (citing *In re Gorman*, 933 F.2d 982, 987 (Fed. Cir. 1991))

Kori Corp. v. Wilco Marsh Buggies & Draglines, 708 F.2d 151, 155 (5th Cir. 1983).

MPEP §2143.03

U.S. Patent No. 6,549,963 to *Sayles*

U.S. Patent No. 6,701,421 to *Elnozahy et al.*

10. Related Proceedings Appendix:

None